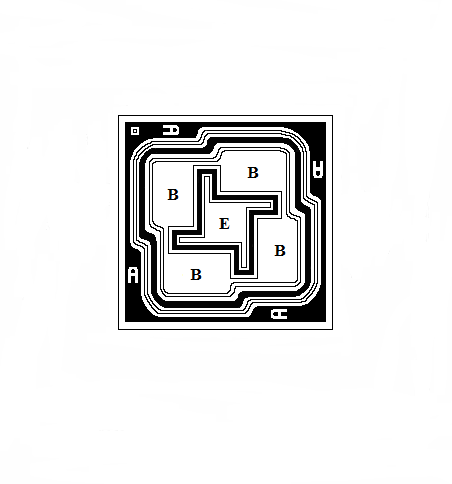
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**.023”**

**.023”**

**D**

**D**

**D**

**D**

**CHIP BACK IS COLLECTOR**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: E = .004” X .004” B = .004” X .0065”**

**Backside Potential: Collector**

**Mask Ref: BDA**

**APPROVED BY: DK DIE SIZE .023” X .023” DATE: 2/7/23**

**MFG: ALLEGRO / SPRAGUE THICKNESS .010” P/N: 2N2904**

**DG 10.1.2**

#### Rev B, 7/19/02